GB 010184
USA
I-II

The Patent Office

INVESTOR IN PEOPLE

The Patent Office
Concept House
Cardiff Road
Newport
South Wales
NP10 8QQ

Priority Letter
2-2/2002

Jc997 U.S. PTO
10/068920
02/07/02

I, the undersigned, being an officer duly authorised in accordance with Section 74(1) and (4) of the Deregulation & Contracting Out Act 1994, to sign and issue certificates on behalf of the Comptroller-General, hereby certify that annexed hereto is a true copy of the documents as originally filed in connection with the patent application identified therein.

In accordance with the Patents (Companies Re-registration) Rules 1982, if a company named in this certificate and any accompanying documents has re-registered under the Companies Act 1980 with the same name as that with which it was registered immediately before re-registration save for the substitution as, or inclusion as, the last part of the name of the words "public limited company" or their equivalents in Welsh, references to the name of the company in this certificate and any accompanying documents shall be treated as references to the name with which it is so re-registered.

In accordance with the rules, the words "public limited company" may be replaced by p.l.c., plc, P.L.C. or PLC.

Re-registration under the Companies Act does not constitute a new legal entity but merely subjects the company to certain additional company law rules.

Signed M Cuskie

Dated 28 November 2001

Patents Form 1/77

Patents Act 1977
(Rule 16)

The Patent Office

THE PATENT OFFICE
A
22 FEB 2001
RECEIVED BY FAX

1/77

22FEB01 E608107-1 D02879
P01/7700 0.00-0104353.8

22 FEB 2001

Request for grant of a patent

(See notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

The Patent Office
Cardiff Road
Newport
Gwent NP9 1RH

1.	Your reference	PHGB010026
2.	Patent application number *(The Patent Office will fill in this part)*	**0104353.8**
3.	Full name, address and postcode of the or of each applicant *(underline all surnames)*	KONINKLIJKE PHILIPS ELECTRONICS N.V. GROENEWOUDSEWEG 1 5621 BA EINDHOVEN THE NETHERLANDS
	Patents ADP Number *(if you know it)*	07419294001
	If the applicant is a corporate body, give the country/state of its incorporation	THE NETHERLANDS
4.	Title of the invention	SEMICONDUCTOR DEVICES
5.	Name of your agent *(if you have one)* "Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*	BRIAN T STEVENS Philips Corporate Intellectual Property Cross Oak Lane Redhill Surrey RH1 5HA
	Patents ADP number *(if you know it)*	07789050001
6.	If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number	Country — Priority Application number *(if you know it)* — Date of filing *(day/month/year)*
7.	If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application	Number of earlier application — Date of filing *(day/month/year)*
8.	Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer "Yes" if:* *a) any applicant named in part 3 is not an inventor, or* *b) there is an inventor who is not named as an applicant, or* *c) any named applicant is a corporate body.* *See note (d))*	YES

Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document.

22 FEB 2001

Continuation sheets of this form	
Description	10
Claims(s)	0
Abstract	0
Drawings	2

If you are also filing any of the following, state how many against each item:

Priority Documents

Translations of priority documents

Statement of inventorship and right to grant of a patent (*Patents Form 7/77*)

Request for preliminary examination and search (*Patents Form 9/77*)

Request for substantive examination (*Patents Form 10/77*)

Any other documents (*Please specify*)

I/We request the grant of a patent on the basis of this application.

Signature Date 22.02.2001.

Name and daytime telephone number of person to contact in the United Kingdom 01293 815294 (Brian T Stevens)

arning

er an application for a patent has been filed, the Comptroller of the Patent Office will consider whether publication or nmunication of the invention should be prohibited or restricted under Section 22 of the Patents Act 1977. You will be ormed if it is necessary to prohibit or restrict your invention in this way. Furthermore, if you live in the United Kingdom, tion 23 of the Patents Act 1977 stops you from applying for a patent abroad without first getting written permission from Patent Office unless an application has been filed at least 6 weeks beforehand in the United Kingdom for a patent for the e invention and either no direction prohibiting publication or communication has been given, or any such direction has n revoked.

es

If you need help to fill in this form or you have any questions, please contact the Patent Office on 0645 500505.

Write your answers in capital letters using black ink or you may type them.

If there is not enough space for all the relevant details on any part of this form, please continue on a separate sheet of paper and write "see continuation sheet" in the relevant part(s). Any continuation sheet should be attached to this form.

If you have answered "Yes" Patents Form 7/77 will need to be filed.

Once you have filled in the form you must remember to sign and date it.

For details of the fee and ways to pay please contact the Patent Office.

Patents Form 1/77

DESCRIPTION

SEMICONDUCTOR DEVICES

This invention relates to semiconductor devices, particularly but not exclusively a power semiconductor switch, having a main current carrying section and a sense current carrying section.

The invention also relates to circuit configurations comprising such a device. The circuit may be used for measuring or modifying or controlling (at least in an abnormal current condition) the conduction of the main current carrying section of the device, in relation to an output from the sense current carrying section.

The invention further relates to switching circuits, switching arrangements and switching schemes comprising such a semiconductor device and/or control circuit, particularly but not exclusively as a high-side switch.

The device is typically an insulated-gate field-effect transistor (MOSFET) or an insulated-gate bipolar transistor (IGBT). The device is usually cellular with, for example a close-packed hexagonal, or square or stripe geometry, and so the main current carrying section and the sense current carrying section are generally referred to hereafter in terms of main cells and sense cells. The control circuit may be integrated monolithically in the same device body (chip) as the transistor, or it may be in a separate circuit body (IC chip) mounted beside the transistor chip, for example in the same device package (encapsulation).

Power MOSFET devices with monolithically integrated control circuits are known. Thus, such devices commercially available from Philips Semiconductors under the trade mark TOPFET include temperature and overload protection functions. TOPFET devices are designed for either high-side or low-side operation, depending on whether used between a power line and the load or the ground line and the load. Such devices are described in the Philips Semiconductors PowerMOS Transistors Data Handbook 1997, for example, and on the web-site http://www.semiconductors.philips.com.

In low-side configured MOSFET designs, current limit and current measure functions have difficulty performing well because of the poor tracking between the MOSFET cells that perform the sensing function (sense cells) and the majority of the MOSFET cells (main cells) that are not monitored. This results from the connection of a small measurement resistor to the source of the sense cells, which thereby makes the sense cells non-representative of the main population.

In high side technologies this can be resolved by feeding the sense cells into a "virtual earth" node, and hence reducing the difference in source voltages between sense cells and non-sensing main cells of the MOSFET. However, the use of a virtual earth technique in a fast current limit control application is particularly challenging from a stability standpoint.

A virtual earth solution cannot be implemented for low-side MOSFET devices, because there is no means to sink the significant sense current, below source potential. Only one strategy was believed to be available in low-side technology. That strategy is to reduce the magnitude of the signal developed across the sense resistor.

The present invention is based on a different approach and understanding by the present inventor. Stated simply, the inventor recognises two components to the "sense ratio" error:

(1) The difference in gate source voltage between the group of sense cells and the cells in the main section of the power MOSFET produces a non-ideal share in response to the transfer function of the component MOSFET cells. This source of error is significant under most conditions.

(2) The non-ideal resistive divider created by the introduction of a small sensing resistor in the source connection of the sense cells also directly generates an error, because it is not matched by a corresponding resistance for the main section of the power MOSFET. This source of error is significant only when the FET is operating fully saturated with a low drain source voltage.

As regards cause (1), the difference in current densities between the sense cells and the main cells can become particularly pronounced at low current densities with the power device running at low levels of enhancement. This is the case when the device is being actively current limited, when the errors from cause (2) are negligible.

As regards cause (2), these errors tend to be worse in devices for "cool running" applications where the drain source operating voltage is very low (i.e. no fault or current limiting conditions).

In accordance with the present invention, there is provided a novel approach that facilitates a correction for errors from (1) and that is applicable generally in control applications where the sense ratio error is a problem. The invention may be applied to monolithically integrated MOSFET devices, for example in the TOPFET (Trade Mark) range, and to discrete MOSFET devices, for example in the SENSEFET range.

According to one aspect of the present invention, there are provided novel semiconductor devices that have separate respective control electrodes for the main section of the device (that carries the main current of the device) and for the sense section (that carries the sense current). For a MOSFET device, the separate respective control electrodes are a separate gate electrode for the main current carrying section, and a separate gate electrode for the sense current carrying section.

The sense current carried by the sense section is indicative and/or representative of the current being carried by the main section. In a MOSFET device in accordance with the invention, the main section and sense section each have their own individual source and gate electrodes. Thus, from this sense section a reference voltage can be derived, with respect to the source electrode of the main section, that is comparable with or equal to or related to the actual gate source voltage appearing between the gate and source electrodes of the reference (sense) section. Because of the separate gate electrode connections of the sense and main sections, this reference voltage can then be used to drive the main section.

Thus, the present invention provides a novel device architecture that is suitable, inter alia, for use in precision current limit and current measure functions. This novel device architecture is realisable using either single chip technologies, for example as in the TOPFET (Trade Mark) range of devices, or using multiple chip technologies, as in the SENSEFET range of devices. Such MOSFETs are particularly beneficial for use as low-side switches.

According to another aspect of the present invention, there are provided novel circuit techniques and circuit configurations that generate an appropriate voltage from the sense section and use that voltage for controlling the main section of the device. Such circuit techniques and circuit configurations can thus be used to facilitate precision current limit and current measure functions on "low-side" configured devices. They may be realised using either single chip or multiple chip technologies. Separate driving of the gates has the additional advantage that it alters the drive requirements for the critical control loop, and makes the engineering of a stable current limit circuit much simpler.

With a MOSFET device in accordance with the invention, the circuit adopted may simply correct the main MOSFET gate drive for the gate-source voltage error incurred by the sense cells, as a result of the inclusion of a sense resistor. In this case, the main MOSFET control loop (with current limit etc.) may be left basically the same. However, the invention also permits a better method of control in which the sense cells are used as a reference structure to be current limited/controlled as desired, and then to drive the main cell array as a "slave unit" with the identical gate source conditions as the reference.

Thus, the present invention can be used to provide both a simple differential correction to the MOSFET main cells (utilising the separate gate connections) and a fully-fledged master-slave arrangement. Accordingly, a variety of circuit aspects are possible with this invention.

The simple differential correction can be of significance where an improved current measure precision is required but a sophisticated current limit facility is not implemented.

The fully-fledged master/slave arrangement has the advantage that the reference device control, which is the critical control loop, is not hampered by the substantial junction capacitances of the main MOSFET section.

These and other advantageous features of the invention are illustrated in specific embodiments of the invention, now to be described with reference to the accompanying drawing Figures 1 to 3.

Figure 1 represents a power MOSFET device in accordance with the invention. This power MOSFET (including its main current carrying section and sense current carrying section) may be formed in a device body (usually a silicon chip) in known manner, except that the MOSFET gates of the main current carrying section and of the sense current carrying section are now separate individual gate electrodes G(1) and G(2) in accordance with the invention. Thus, although the main current carrying section and sense current carrying section of previously known MOSFETs have separate source electrodes, their gate electrodes are common.

The MOSFET may be, for example, of the trench-gate type or of the DMOS (planar surface MOS) type. Published PCT patent application WO-A-00/62422 (our ref. PHB34338) is, inter alia, an example of the fabrication of a trench-gate power MOSFET with main current carrying and sense current carrying sections, but without the separate individual gate electrodes in accordance with the present invention. The whole contents of WO-A-00/62422 are hereby incorporated as reference material.

A variety of cellular layouts may be adopted for the power MOSFET (both its main current carrying section and its sense current carrying section), for example a close-packed hexagonal, or square or stripe geometry.

Traditionally the sense cell structure has been manufactured with cells in the same MOSFET body with a separate source electrode/terminal (2). The present invention provides also a separate gate electrode G(2). Thus, the invention can exploit the advantages of separate gate and source connections, whilst still maintaining an integrated structure for the main and sense sections

so as to ensure thermal and constructional matching. Usually the drain electrode will be common to the sense and main sections, as well as the drain region and drain drift region. The transistor-body regions (channel region) and source regions of the main and sense sections can still be formed in the same process steps, and so may the electrode metallisation. Only the layout pattern of the gate electrodes G(1) and G(2), their metallisation and connections (if integrated) needs to be changed so as to separate electrically the gate electrodes G(1) and G(2) of the main and sense sections.

Thus, even for the specific circuit embodiments illustrated in Figures 2 and 3, a variety of MOSFET device configurations are possible in accordance with the invention. These configurations depend on the choice of various factors such as:

- whether the control circuit is integrated in and/or on the same device body as the MOSFET itself, so producing a monolithic integrated device as in the TOPFET (Trade Mark) range;
- whether the control circuit (when not integrated in and/or on the device body) is nonetheless still encapsulated in the same package as the MOSFET device body, so producing a hybrid device or device module;
- whether the device package encapsulates only the MOSFET device body, so producing a discrete device as in the so-called SENSEFET range.

Thus, the MOSFET device body may have separate bond pads connected respectively to the separate individual gate electrodes G(1) and G(2) of the main section and of the sense section of the MOSFET, when the control circuit is not integrated in the MOSFET chip. In this case, the device package may have separate terminal pins connected to these separate bond pads of the gate electrodes G(1) and G(2) of the main section and sense section, when the control circuit is not encapsulated in the device package.

The device may be a discrete device in the so-called SENSEFET range, but having separate respective gate terminals G(1) and G(2) for its main

current carrying section and its sense current carrying section, in accordance with the invention.

However, the device package may encapsulate the control circuit, when the control circuit is integrated in and/or on the MOSFET chip or when the control circuit is formed in one or more circuit bodies (IC chips) mounted side-by-side with the MOSFET chip. The separate individual gate electrodes G(1) and G(2) of the main section and of the sense section of the MOSFET can be directly connected with respective elements of the control circuit by means of conductor tracks, when at least parts of the control circuit are integrated in and/or on the MOSFET chip. Otherwise, bond wires may be connected between bond pads of the MOSFET chip and bond pads of a control circuit chip.

Figure 2 illustrates a specific embodiment of a master-slave arrangement in accordance with the present invention. The sense cells function as reference cells. These reference cells are operated in a self-contained control loop, engineered to deliver the final current limit/ current measure functionality.

A reference voltage is then generated, with respect to the main MOSFET array source terminal, that is equal to the actual gate source voltage that appears between the gate and source connections of the reference (sense) cell array. This is then utilised by a high-speed buffer/driver module to drive the main MOSFET array.

Although not shown in Figure 2, it is also advantageous to implement some protection functions (such as over-voltage) on the main MOSFET array only.

The proposed arrangement has several advantages:

Thus, significantly improved current limit precision is achievable for the following reasons:

The error in the gate-source voltages applied to reference (sense) cell array and the main MOSFET array is now a function of the RMS sum of the offset voltages of 3 precision amplifiers of Figure 2, rather than the amplitude

of sense current signal. This can result in a higher level of precision for low-side current limit and current measure applications, for both MOSFETs in the TOPFET (Trade Mark) range and for other MOSFETs.

The most difficult control loop (i.e. the high speed, high closed loop gain amplifier used for the current limit function) is now freed from the constraint of having to drive the high junction capacitance of a power FET. This amplifier should ideally be configured as an "integrator" at high speeds, to maximise the stability when driving inductive loads. Configuring the amplifier as an integrator, for all closed loop gains greater than 1, controls the phase shift from the amplifier to 90°, and hence maximum phase shift in the closed loop under all load conditions to less the 180°. Hence the best possible stability is assured.

The driver module ("slave") responsible for driving the high gate capacitance of the power FET now has a much easier task since the stability analysis of its, buffer type, control loop is a lot less demanding.

The corrected reference generator is generating a new reference for the main MOSFET array by forcing a current to flow through two equal resistors R2 and R3. The reference generator control amplifier adjusts this current such that the voltage developed across R2 is equal to the voltage across the sense resistor R1. Therefore, the voltage across the matched resistor R3 must also be equal to the voltage across the sense resistor. This means that the voltage that appears on the +ve input of the slave control loop amplifier, with respect to the source terminal, is equal to the gate-source voltage that has been set on the reference cells.

Figure 3 illustrates an alternative architecture, in which the corrected reference generator and the slave control amplifier are combined into one circuit element. This is a simpler circuit configuration, but with an overall performance that will be somewhat worse for all conceivable technologies and components sets. The poorer performance results from the poor common-mode rejection ratio of this circuit and the multiplication of the amplifier input offset voltage. However it will be quite adequate for many applications.

The above disclosure of the invention is primarily in terms of a "low-side" switch. However, features of the present invention may also be applied to a "high-side" switch and are particularly advantageous for a fast current-limit control application of the "high-side" switch.

The above disclosure of the invention is mainly written in terms of a MOSFET type of device. However the invention may be applied to other types of semiconductor device, for example to other FETs or to bipolar transistors or to IGBTs.

In the case of other types of field-effect transistor, for example, the insulated gate may be replaced by so-called Schottky gate technologies. In this case, the gate dielectric layer is omitted and the conductive gate electrode forms a Schottky barrier with the lowly-doped channel-accommodating area of the transistor body region. In another FET type, the source regions could be formed as Schottky contact regions rather than as dopant diffused or implanted regions.

A bipolar transistor has emitter and collector (instead of source and drain), and a base (instead of the gate). An IGBT has cathode and anode (instead of source and drain), but its control electrode is still an insulated gate. Each of these device types can be configured with a main current carrying section and a sense current carrying section, the current paths of which extend between first and second electrodes of the device. The second electrode (drain or anode or collector) is usually common to both the main and sense sections. The first electrode (source or cathode or emitter) of the main section is separate from that of the sense section, so that a sense current output can be derived from the separate first electrode of the sense section. The main and sense sections have individual separate respective control electrodes in accordance with the present invention.

From the present disclosure, other modifications and variations will be apparent to persons skilled in the art. Such modifications and variations may

involve other features which are already known in the art and which may be used instead of or in addition to features already disclosed herein.

No specific patent claims have yet been formulated in this patent application to particular combinations of features. However, it should be understood that the scope of the disclosure of the present patent application includes any and every novel feature or combination of features disclosed herein either explicitly or implicitly and together with all such modifications and variations, whether or not relating to the main inventive concepts disclosed herein and whether or not it mitigates any or all of the same technical problems as the main inventive concepts.

The applicants hereby give notice that patent claims may be formulated to such features and/or combinations of such features during prosecution of the present patent application or of any further application derived or claiming priority therefrom.

1/2

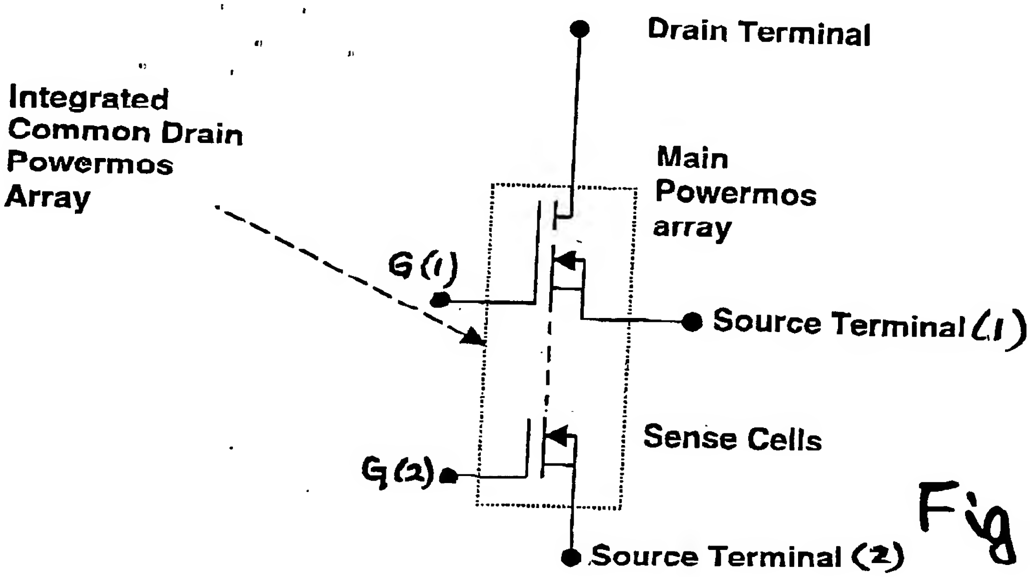

Fig.1.

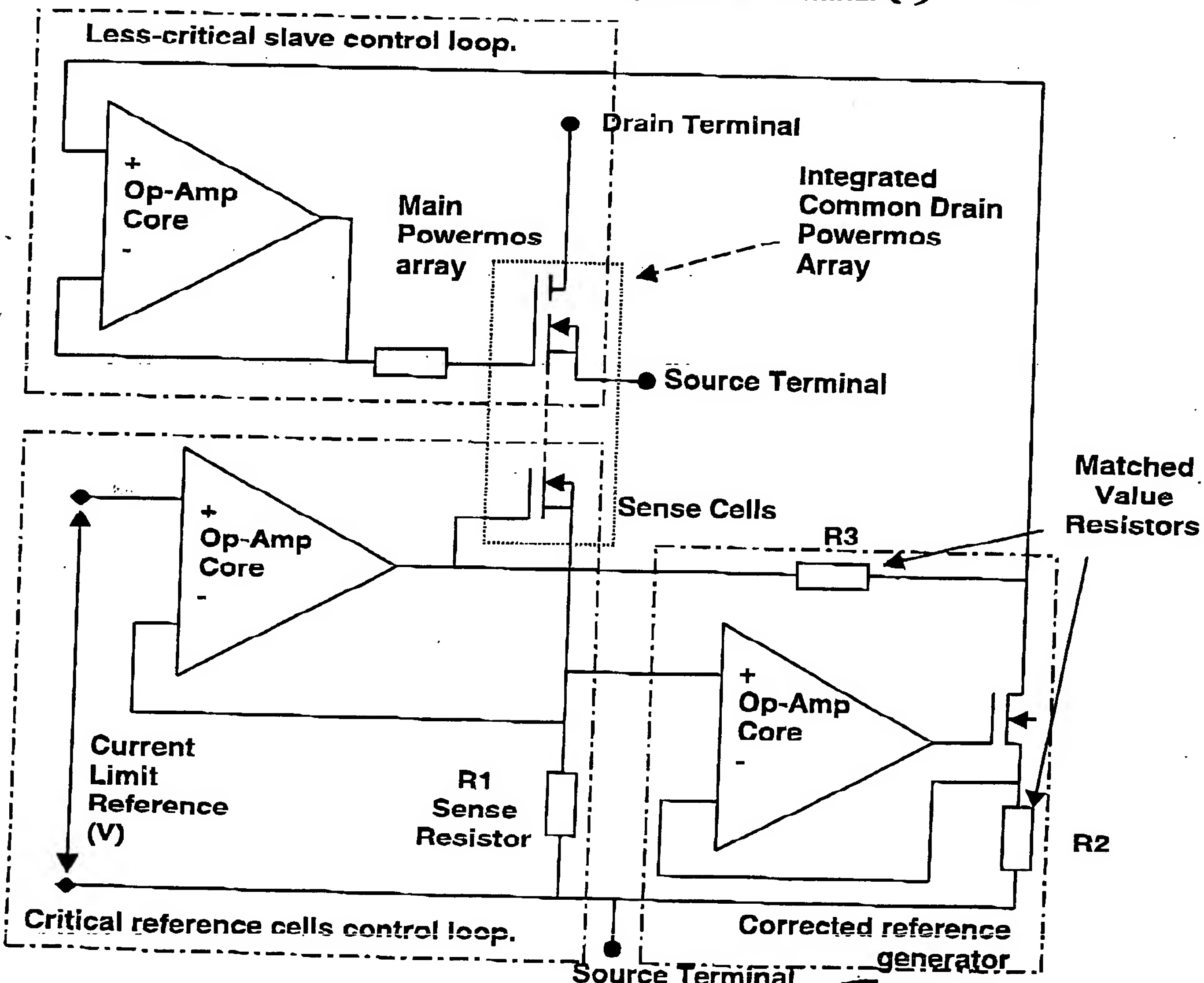

Fig.2.

PHGB010026

2/2

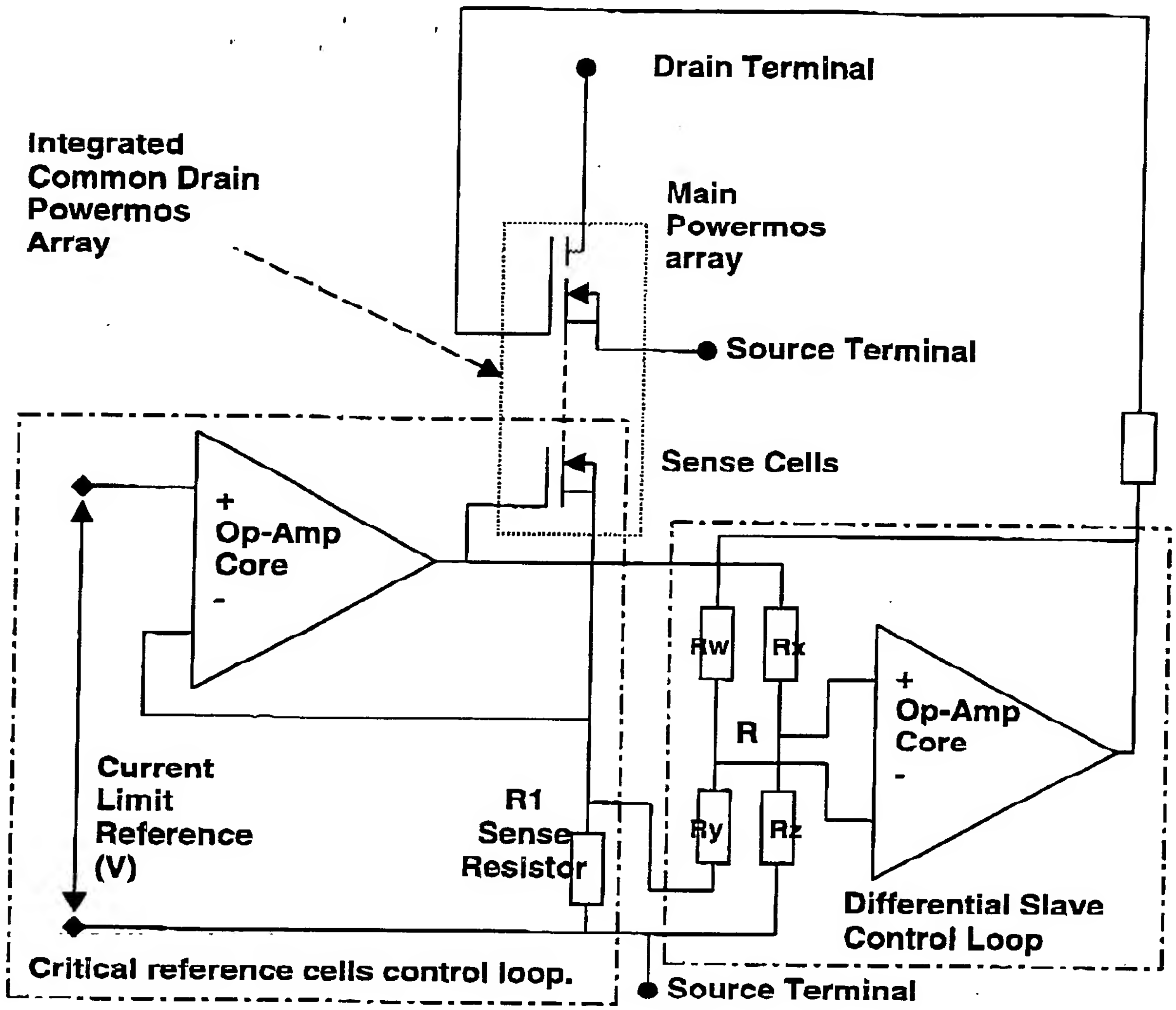

Fig. 3.

PHGB010026.